

Fig. 1 Prior art

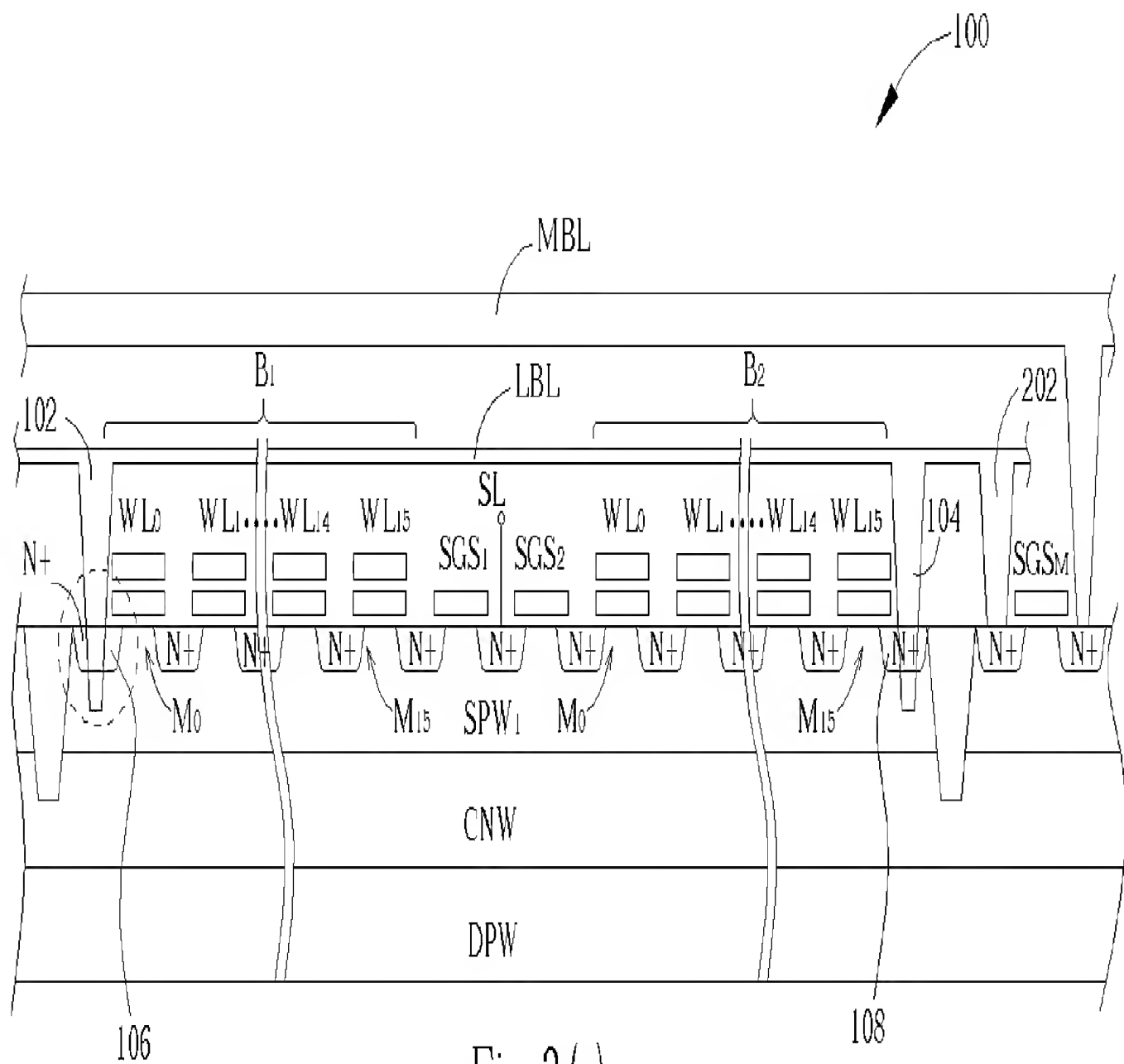


Fig. 2 (a)

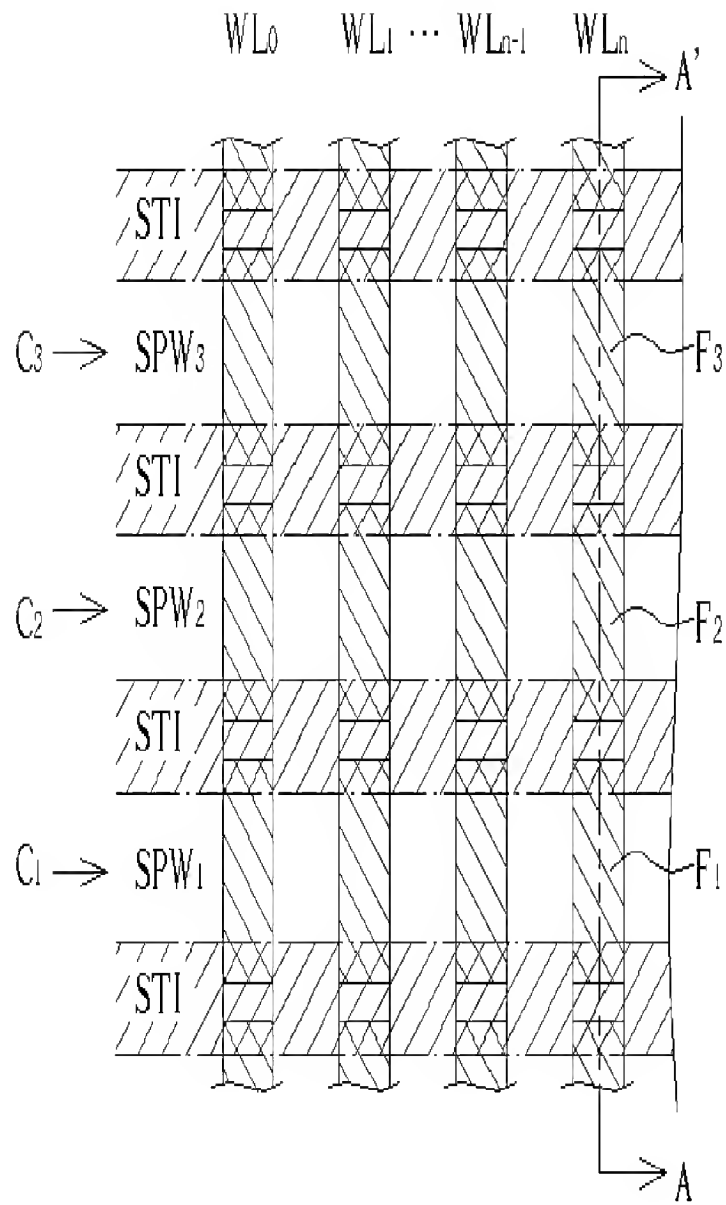


Fig. 2 (b)

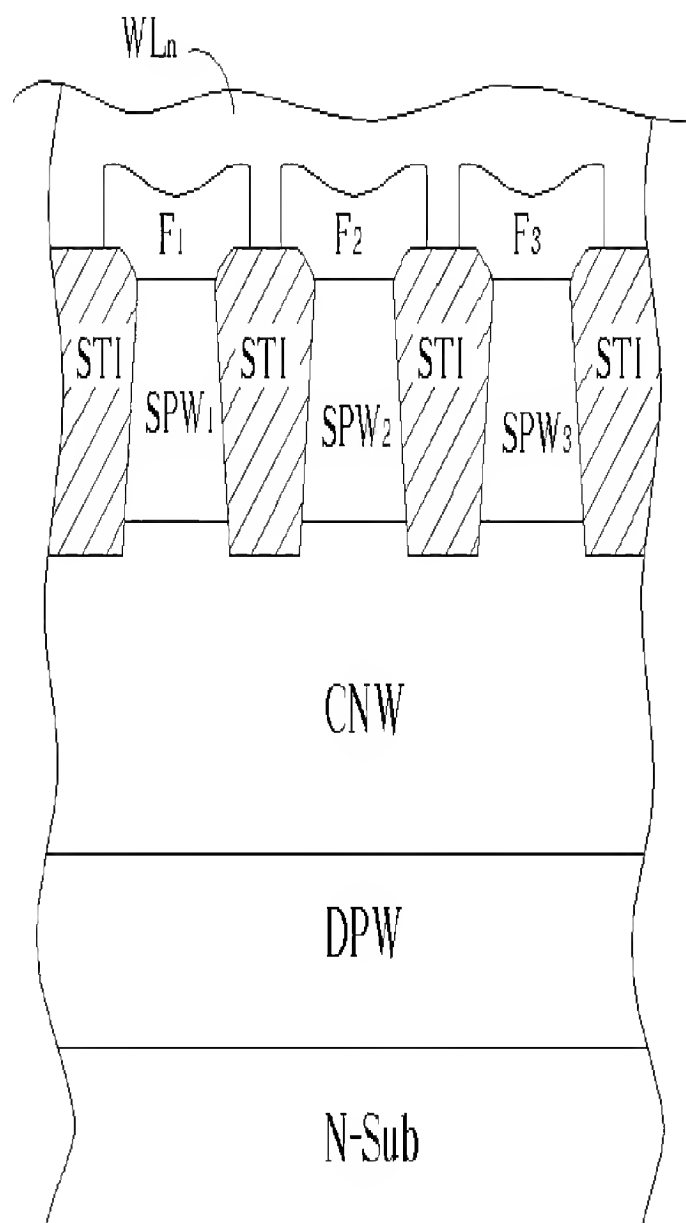


Fig. 2 (c)

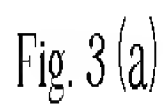


Fig. 3 (a)

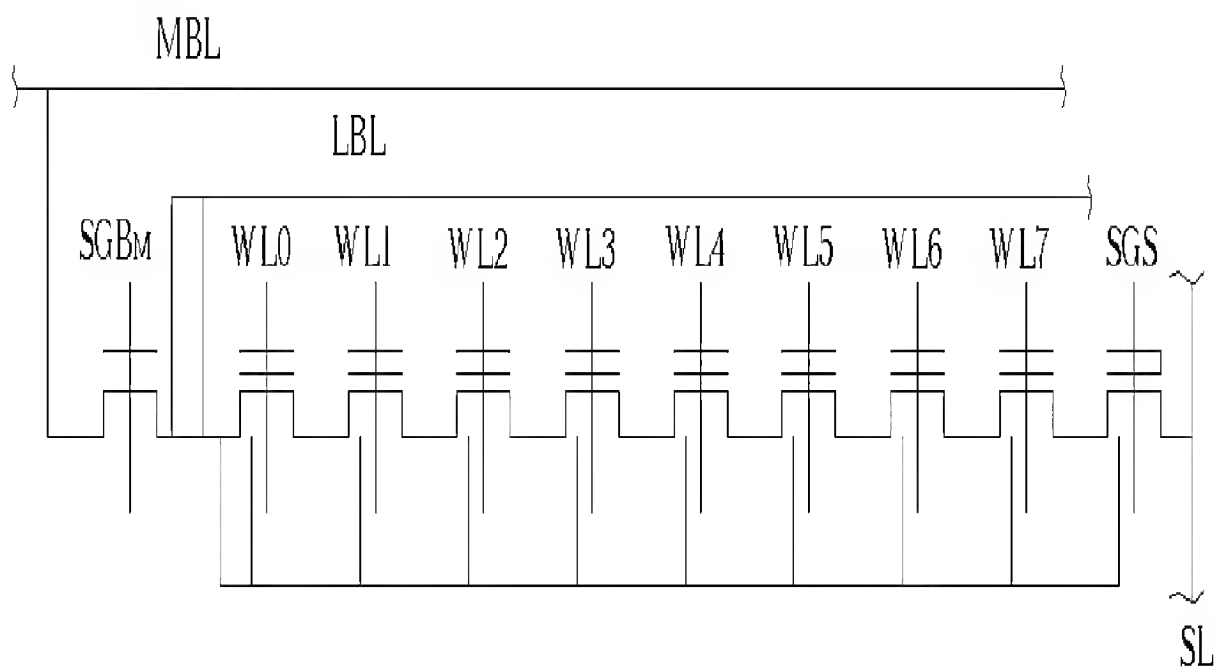


Fig. 3(b)

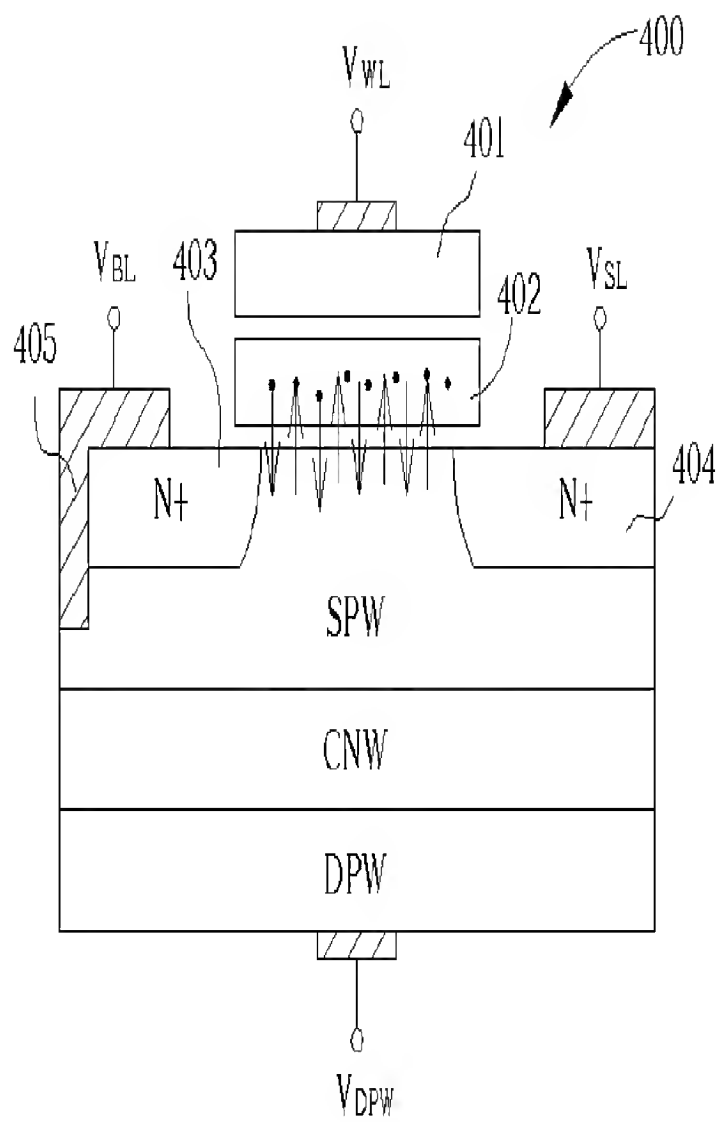


Fig. 4 (a)

	V_{BL}	V_{WL}	V_{SL}	V_{DPW}
Program	5V	-10V	Float	0V
Erase	Float	10V	-8V	-8V
Read	0V	0V	1.5V	0V

Fig. 4 (b)

ERASURE OPERATION

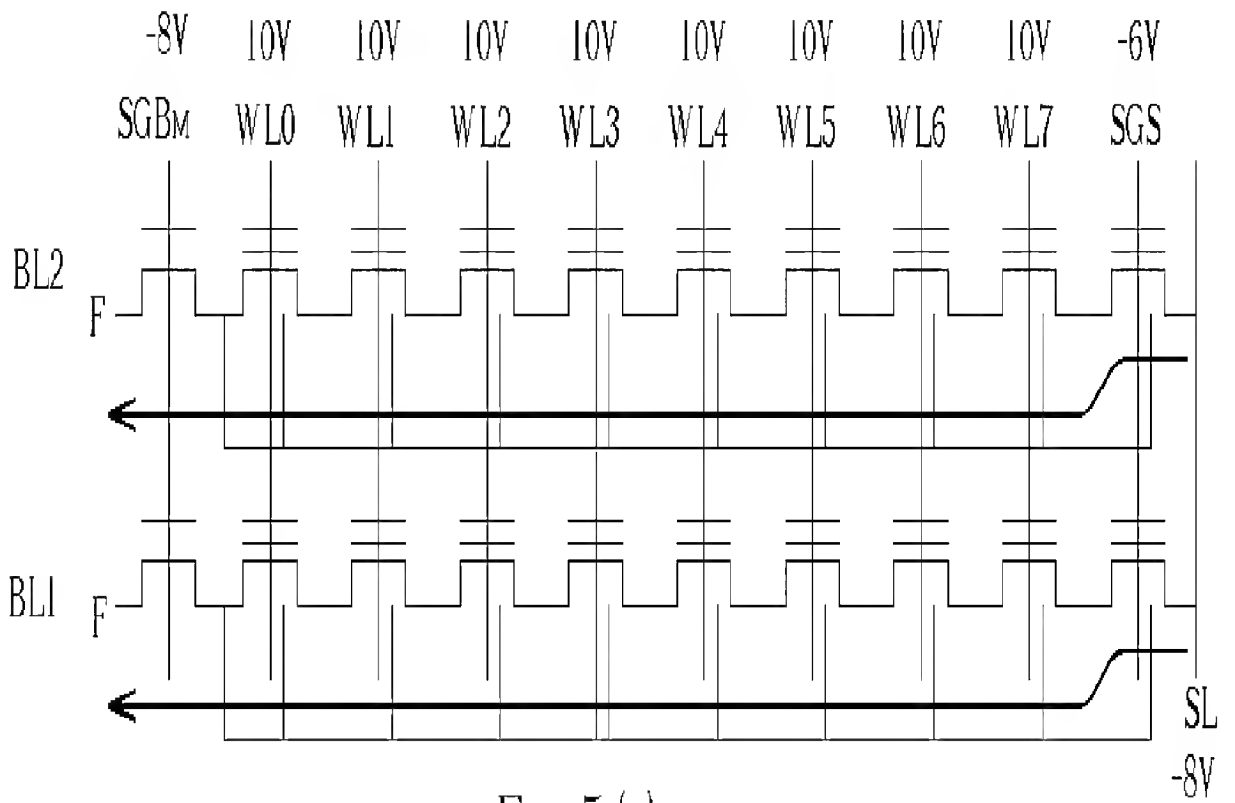
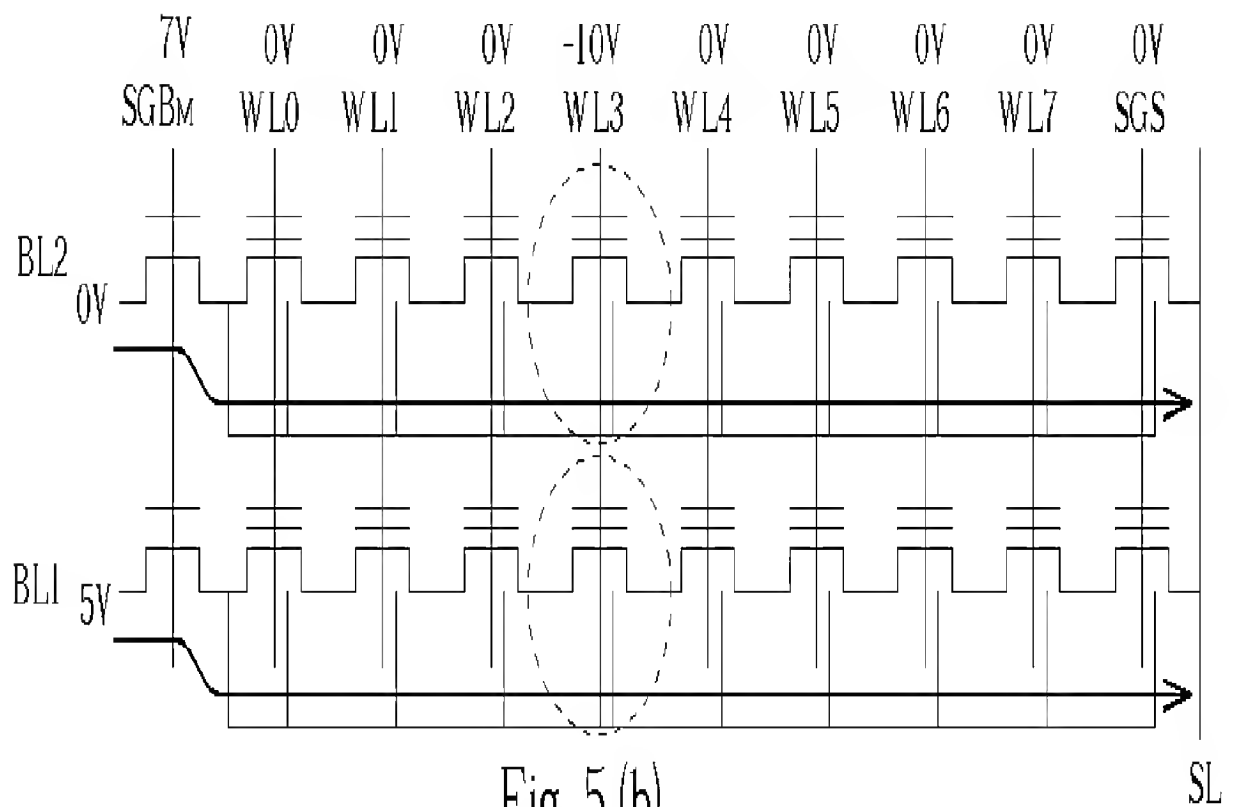


Fig. 5 (a)

PROGRAMMING OPERATION



READ OPERATION

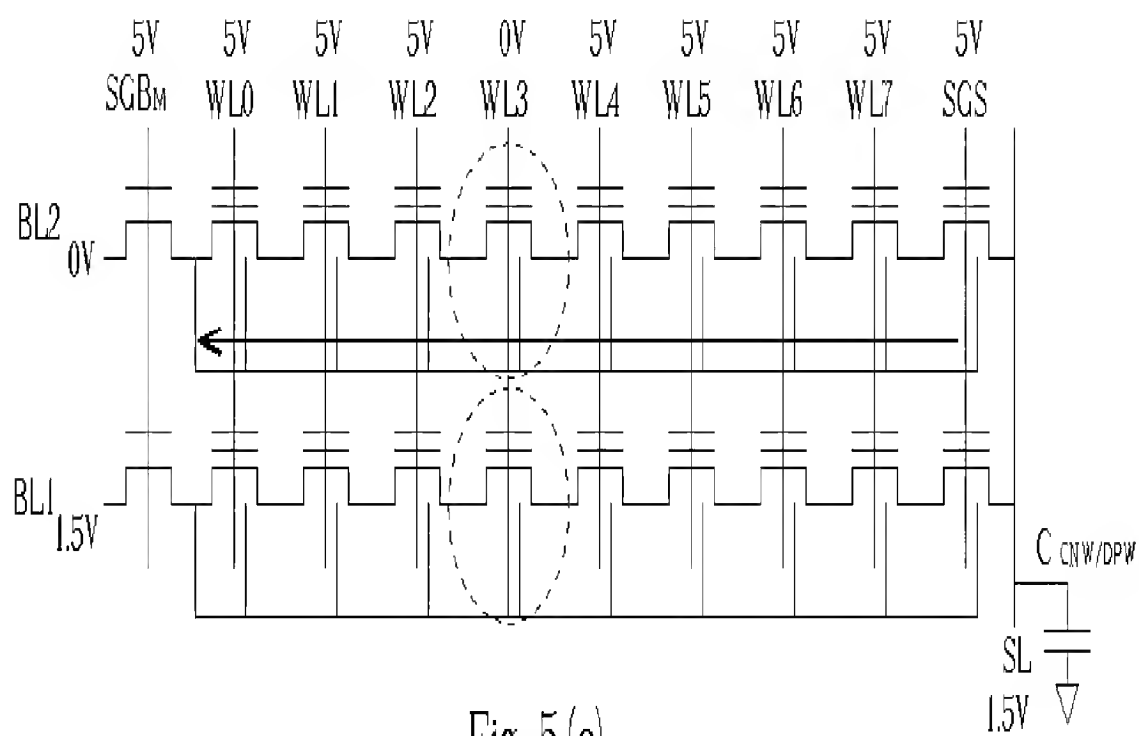


Fig. 5 (c)

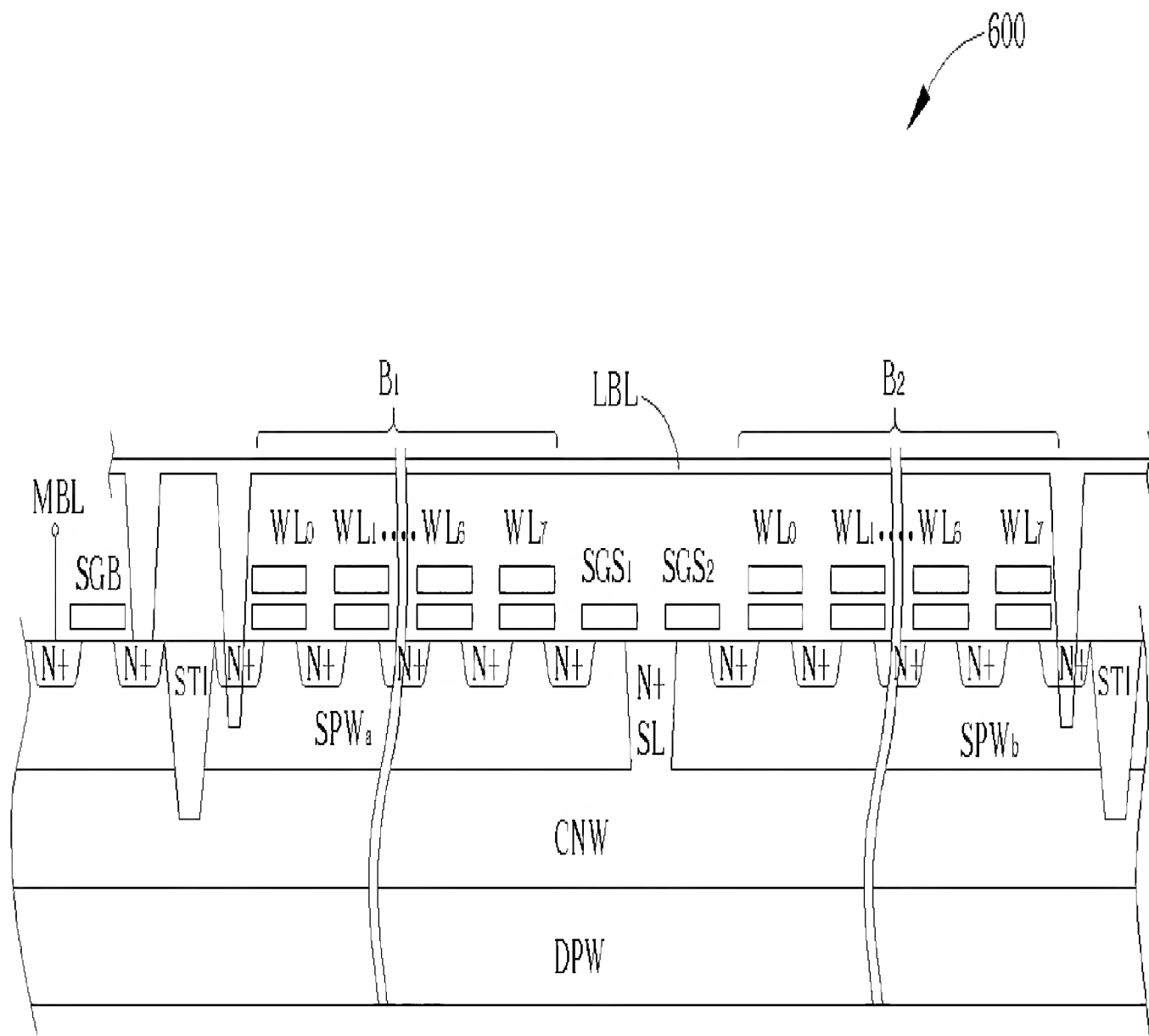


Fig. 6

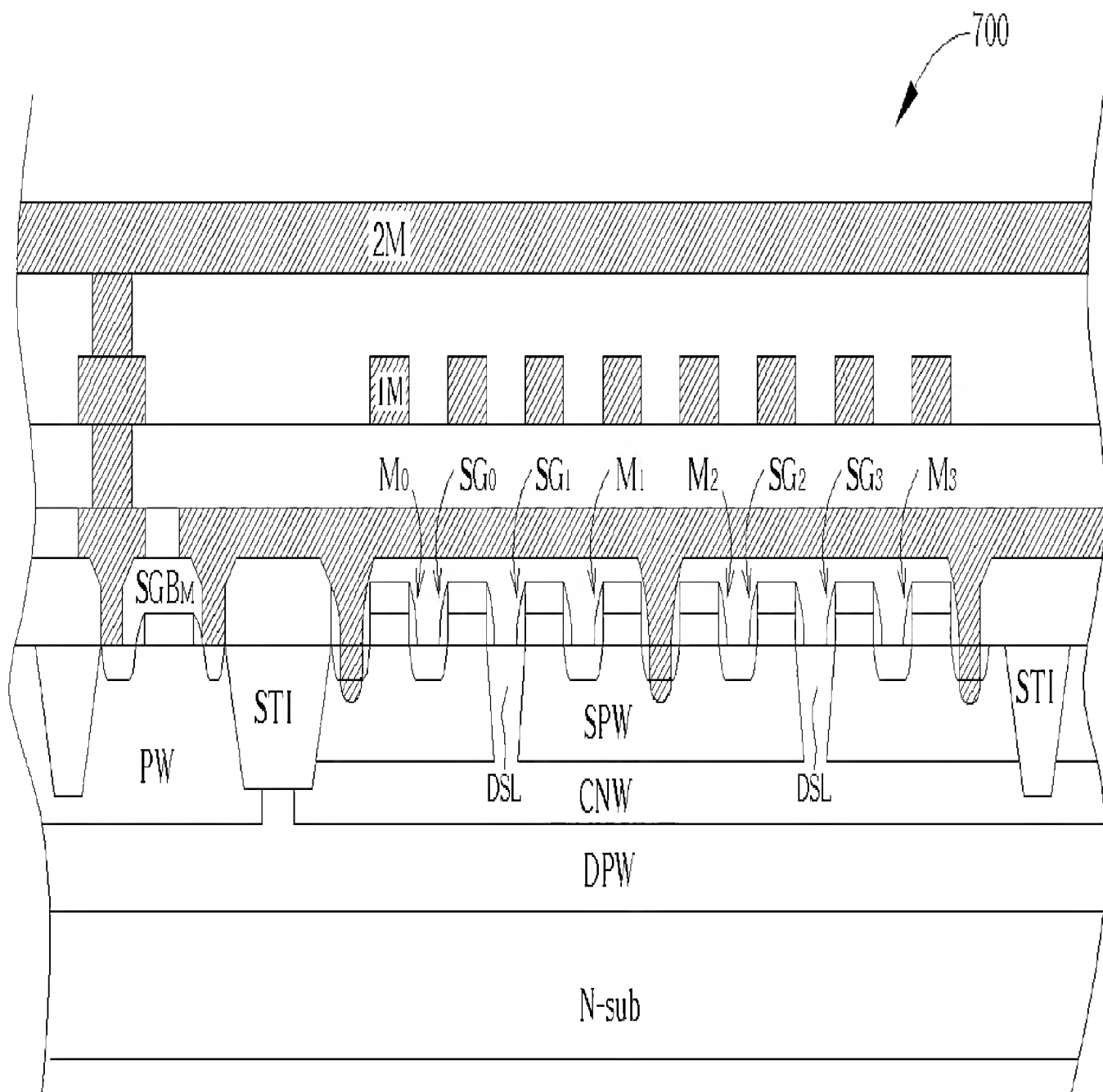


Fig. 7 (a)

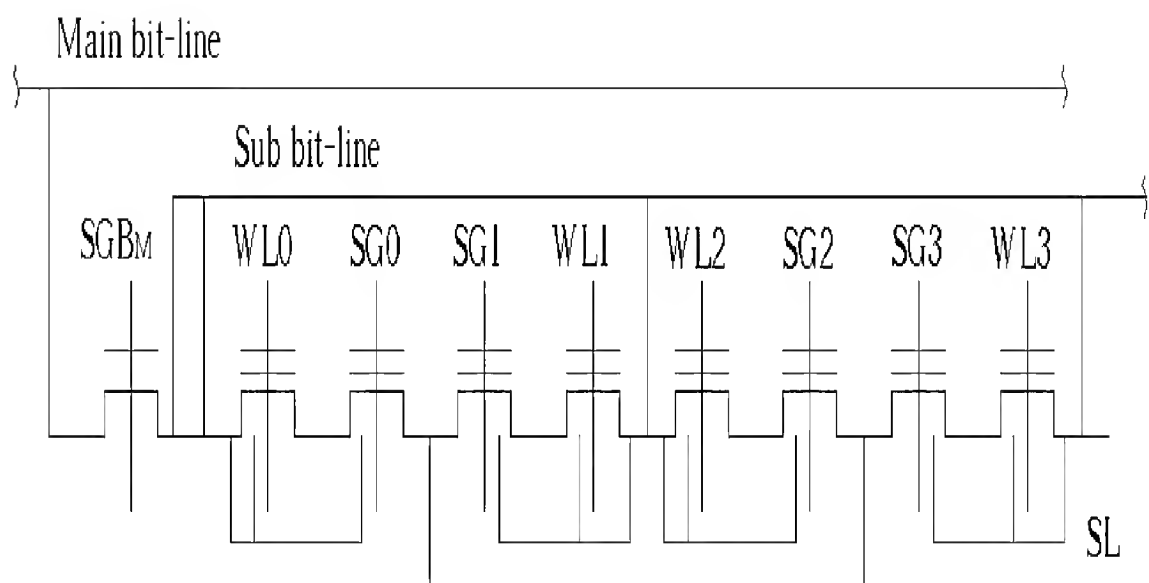


Fig. 7 (b)

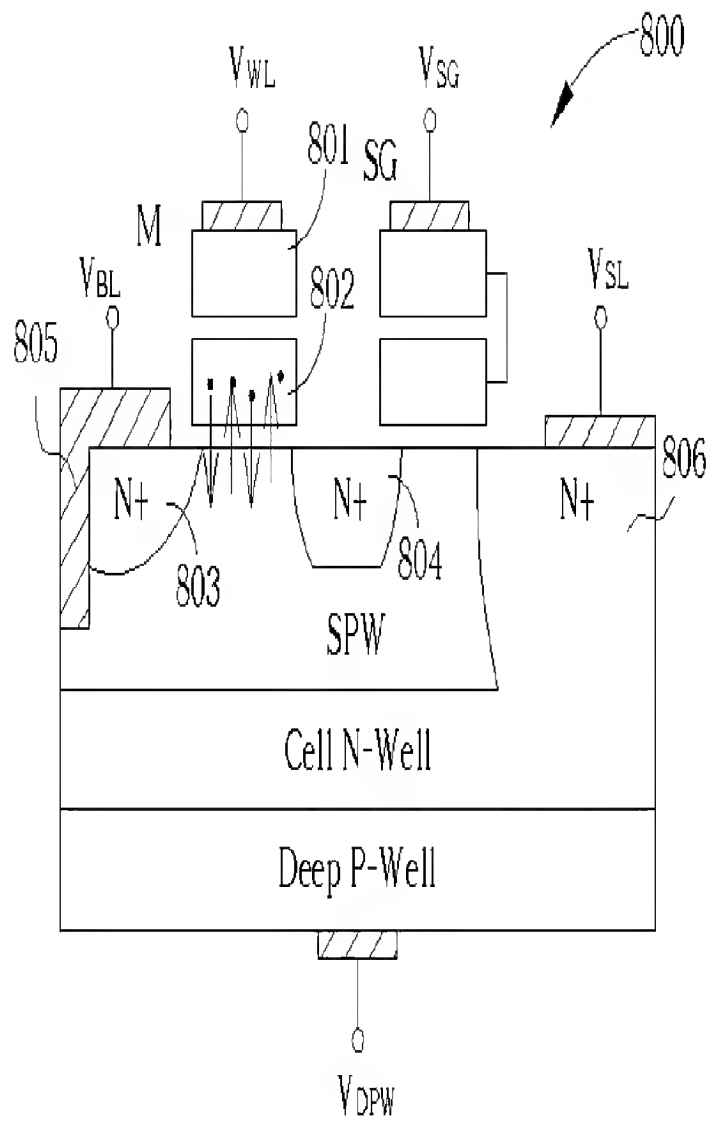


Fig. 8 (a)

	V_{BL}	V_{WL}	V_{SG}	V_{SL}	V_{DPW}
Program	5V	-10V	0V	Float	0V
Erase	Float	10V	-6V	-8V	-8V
Read	0V	0V	5V	1.5V	0V

Fig. 8 (b)

ERASURE OPERATION

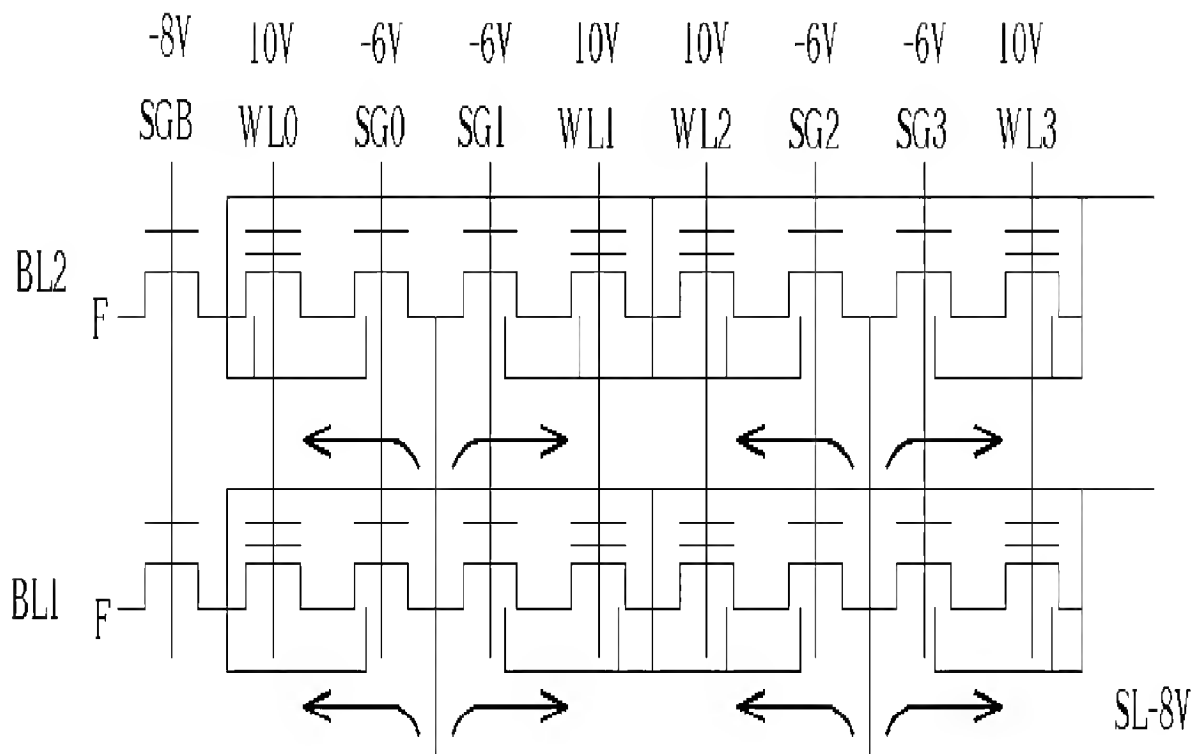


Fig. 9 (a)

PROGRAMMING OPERATION

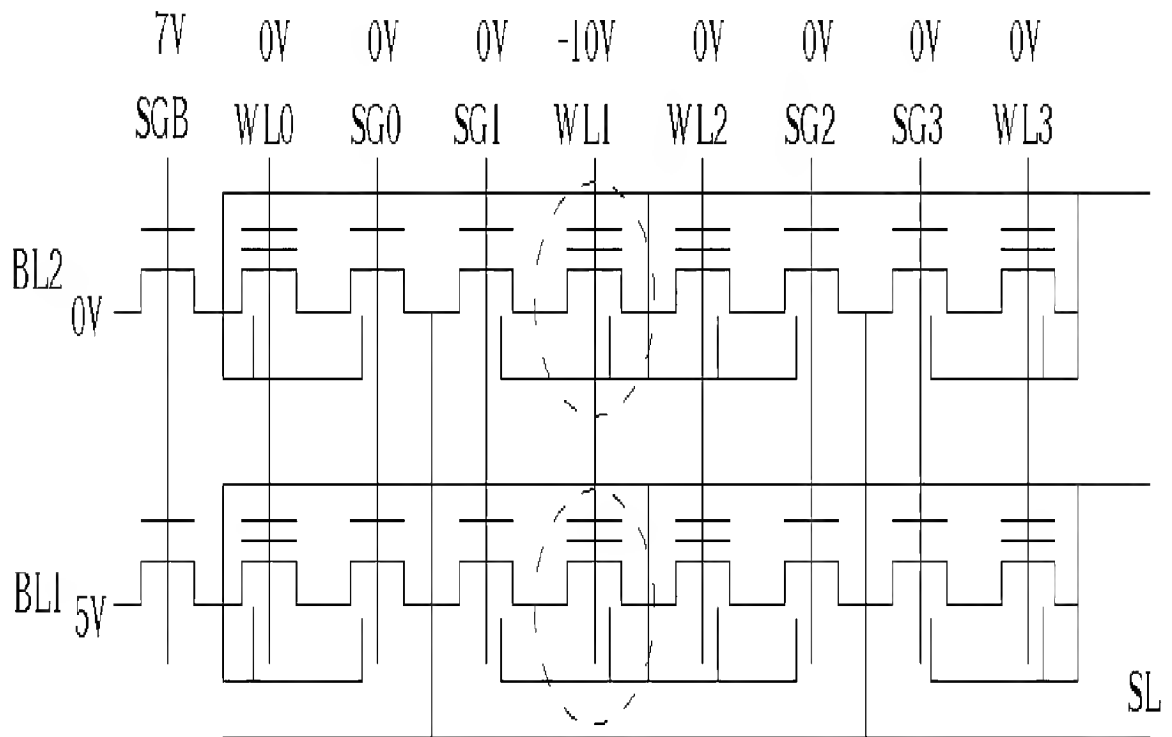


Fig. 9 (b)

READ OPERATION

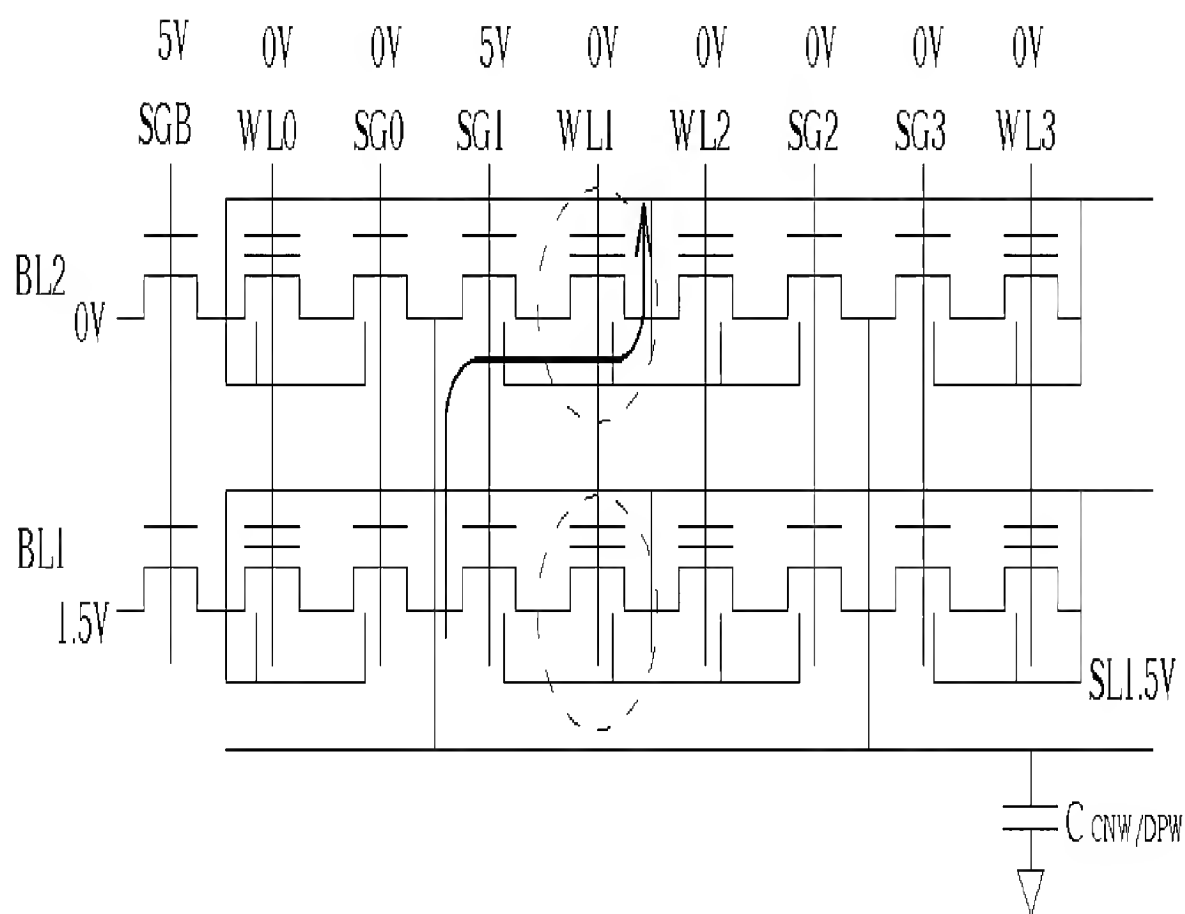


Fig. 9 (c)

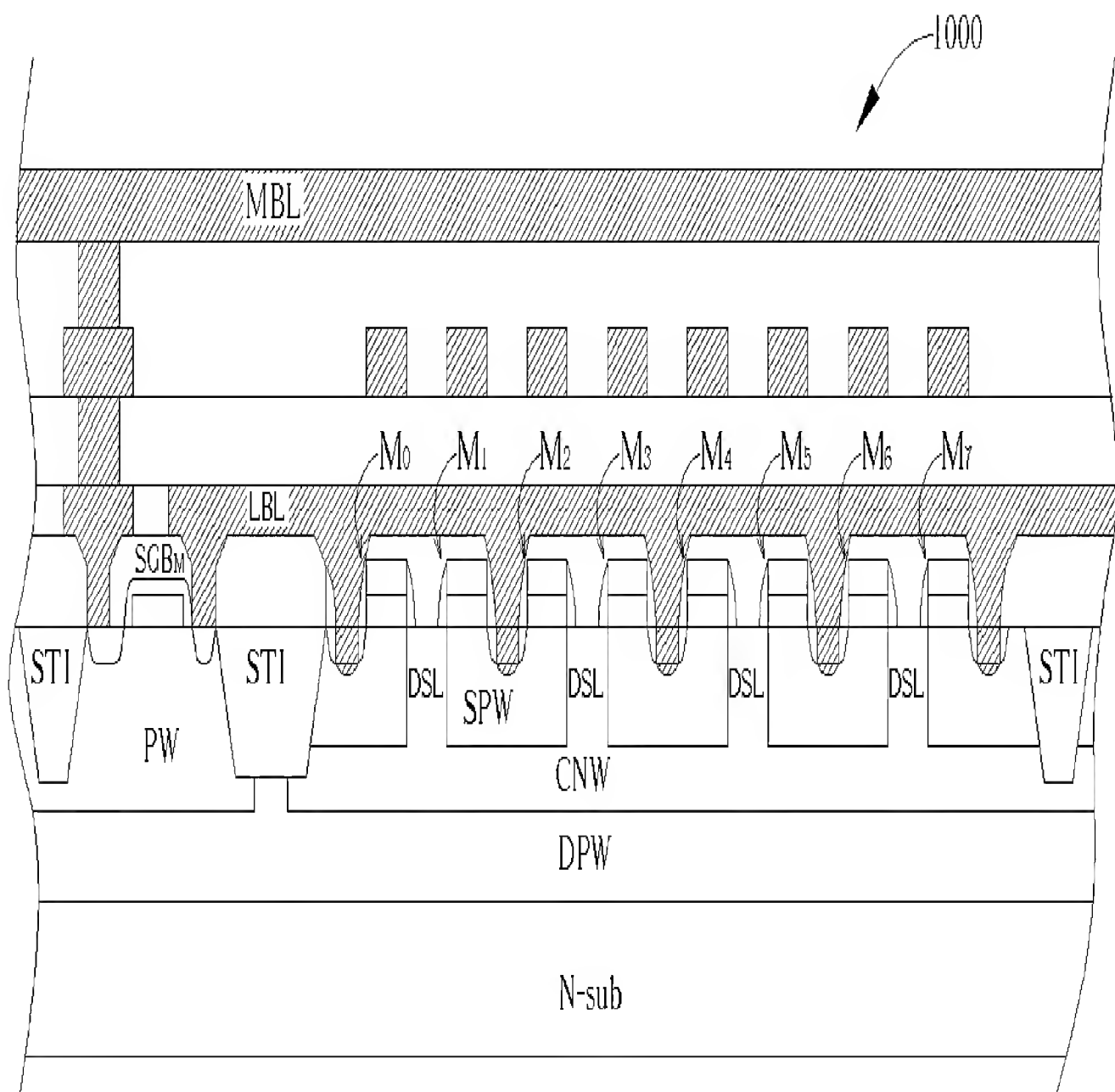


Fig. 10 (a)

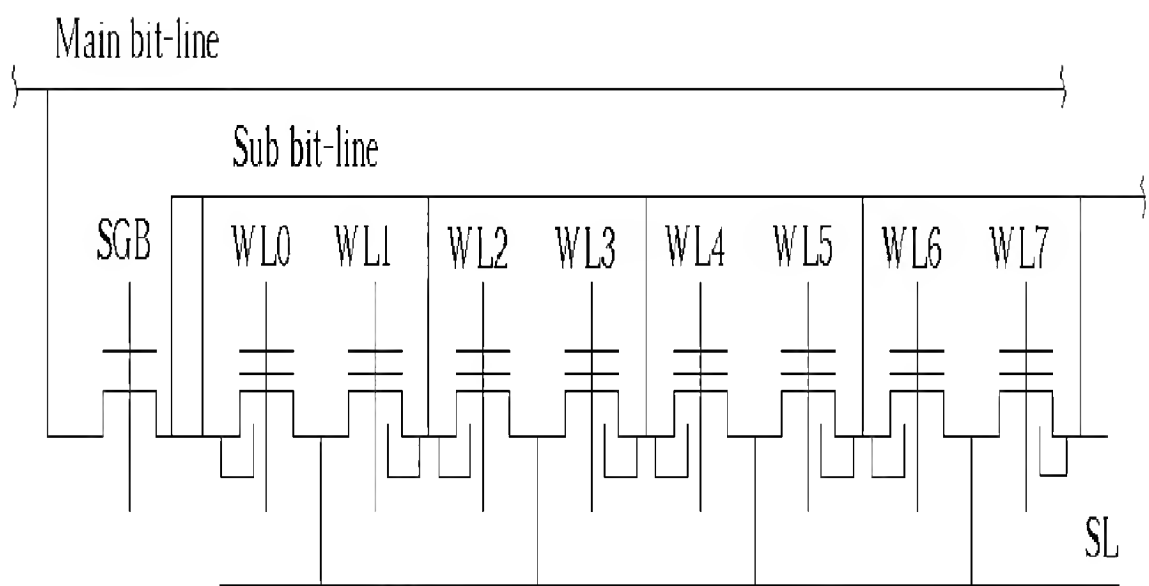


Fig. 10 (b)

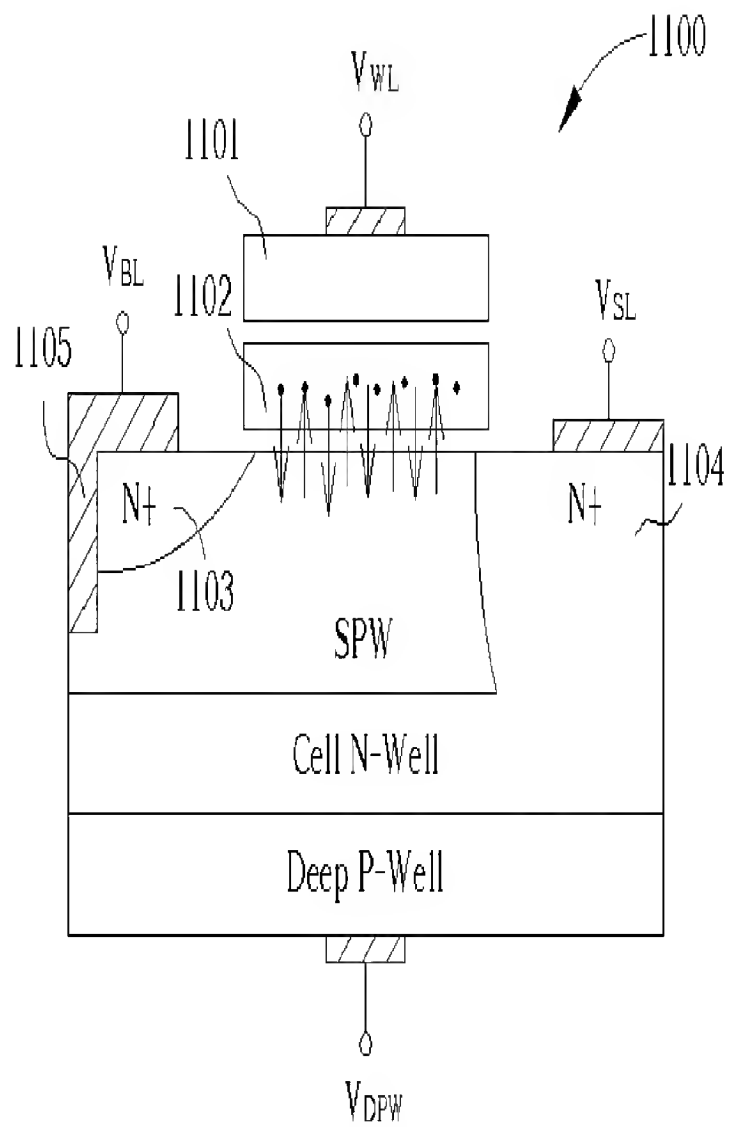


Fig. 11 (a)

	V_{BL}	V_{WL}	V_{SL}	V_{DPW}
Program	5V	-10V	Float	0V
Erase	Float	10V	-8V	-8V
Read	0V	4V	1.5V	0V

Fig. 11 (b)

ERASURE OPERATION

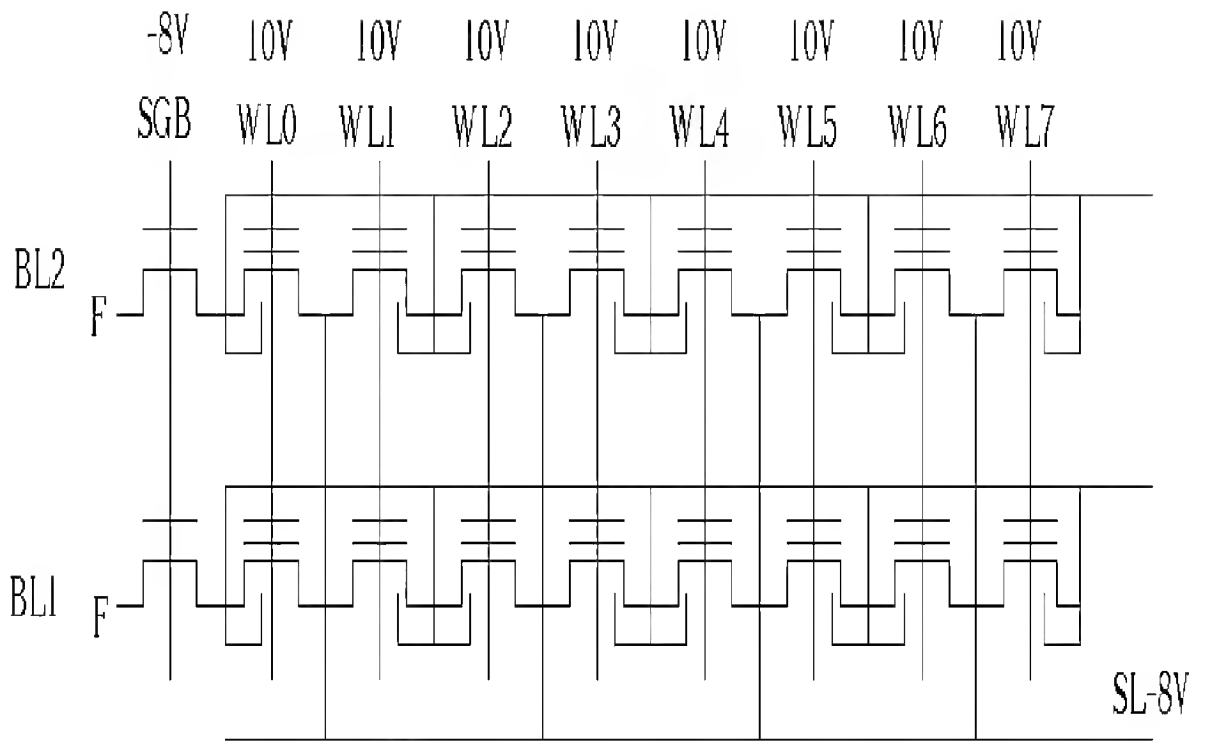


Fig. 12 (a)

PROGRAMMING OPERATION

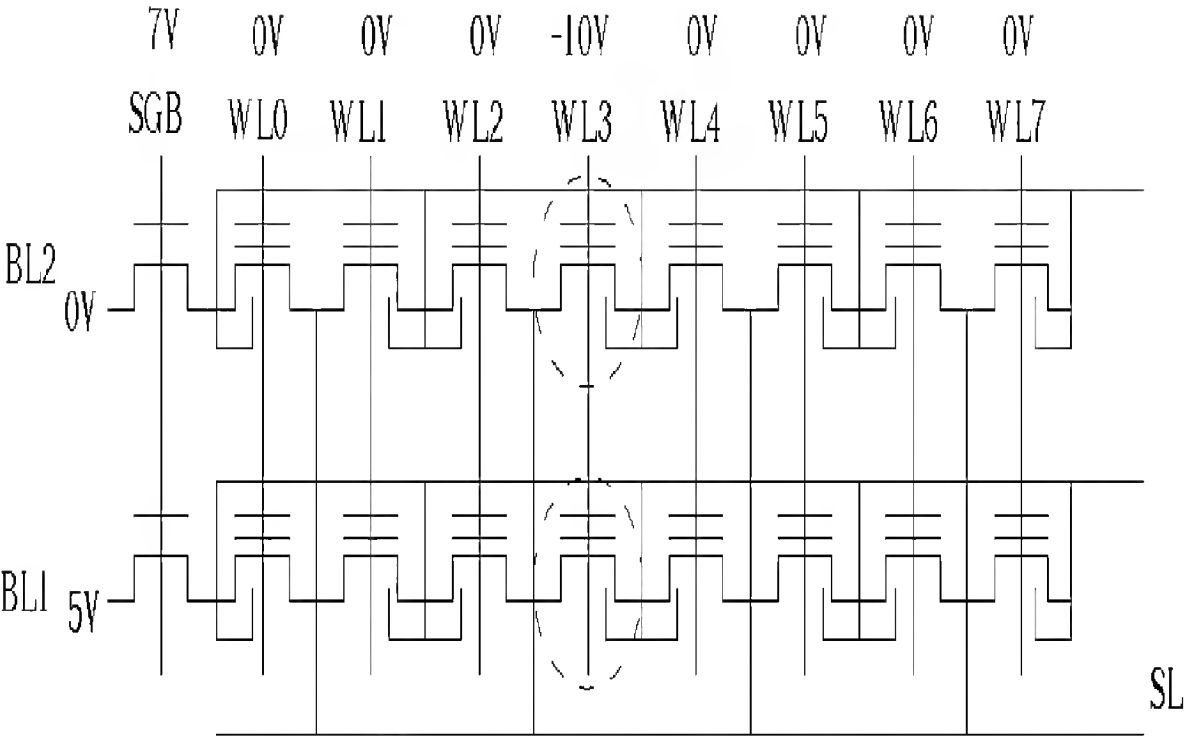


Fig. 12 (b)

READ OPERATION

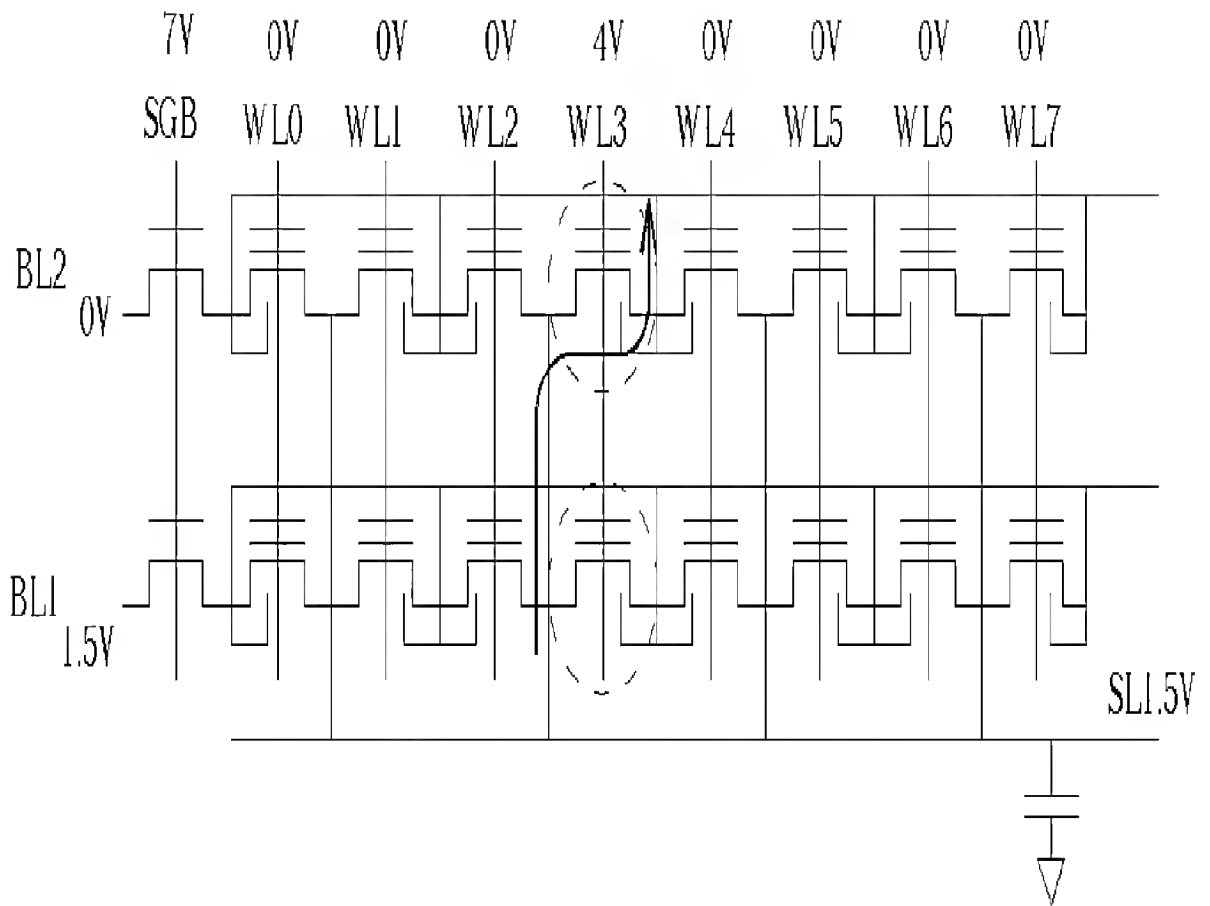
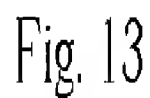






Fig. 12 (c)



-  PN Junction
-  Memory cell
-  Source line selection transistor
-  Deep N^+ well

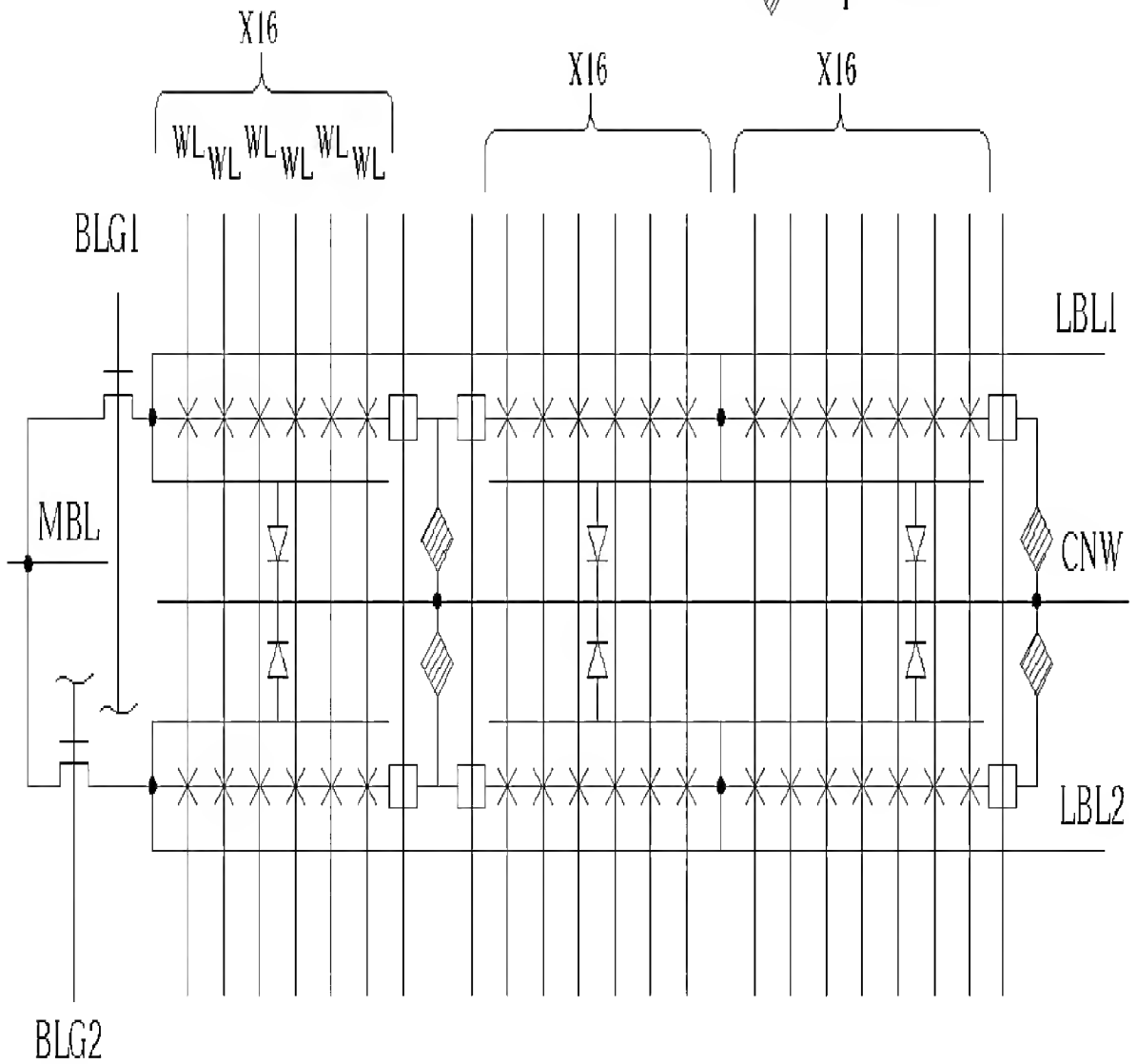


Fig. 14

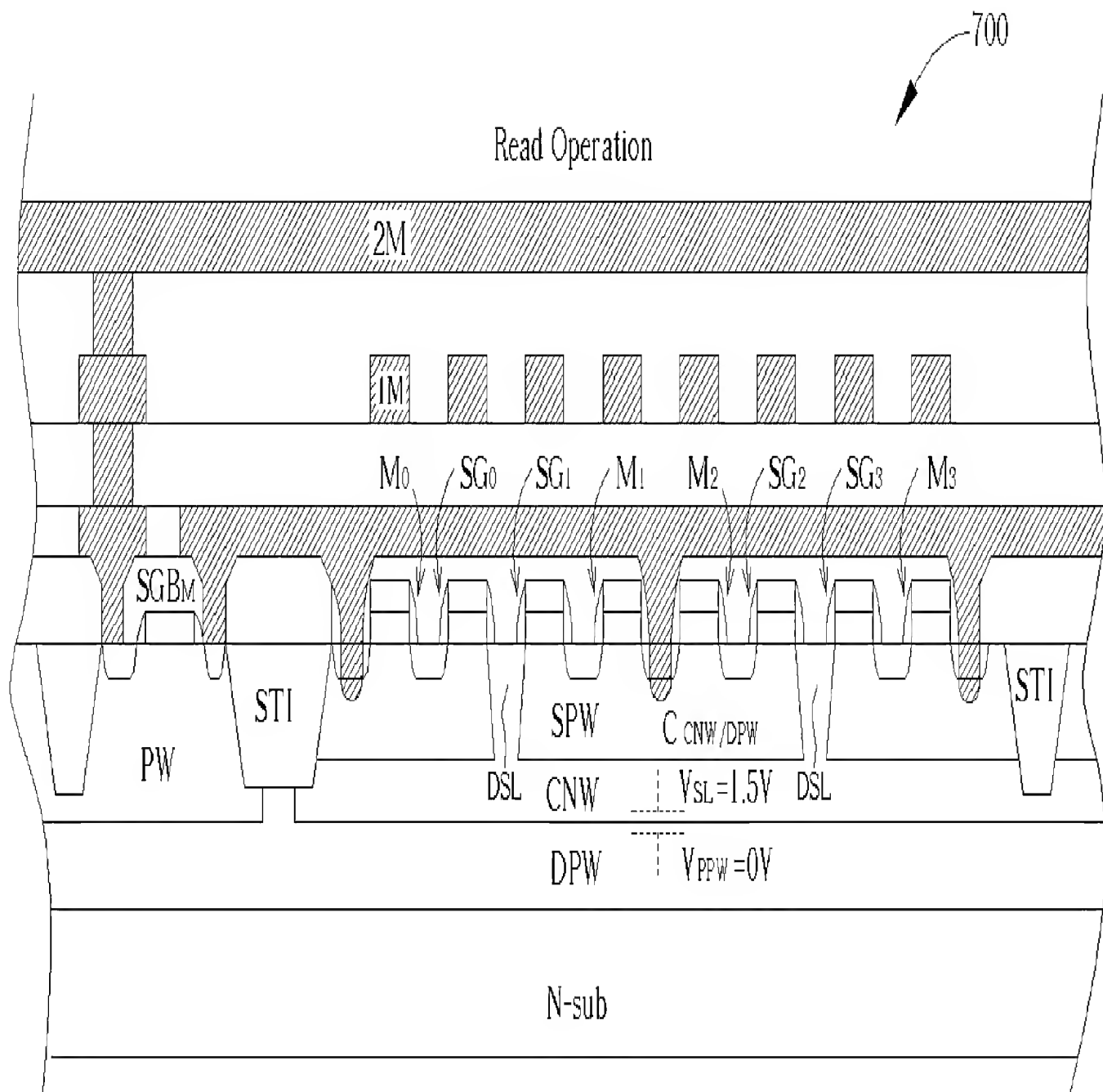


Fig. 15